Docket No.: 61282-044 **PATENT** 

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Customer Number: 20277

Shinichi Abe Confirmation Number:

Group Art Unit:

Serial No.:

Filed: October 31, 2003 Examiner:

SEMICONDUCTOR INTEGRATED CIRCUIT AND INTERRUPT REQUEST OUTPUT METHOD For:

**THEREOF** 

## **CLAIM OF PRIORITY**

Mail Stop CPD Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 35 U.S.C. 119, Applicants hereby claim the priority of:

Japanese Patent Application No. JP 2002-320215, filed on November 1, 2002.

cited in the Declaration of the present application. A certified copy will be filed in due course.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

600 13<sup>th</sup> Street, N.W. Washington, DC 20005-3096 (202) 756-8000 MEF:gav Facsimile: (202) 756-8087

Date: October 31, 2003